REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-15 are presently active in this case, Claims 1 and 10 having been amended and Claim 15 having been added by way of the present Amendment.

The amendments to the claims are fully supported by the disclosure of the present application, for example, on page 6, lines 1-18.

In the outstanding Official Action, Claims 1-5 and 9 were rejected under 35 U.S.C. 103(a) as obvious of Gerber et al. (U.S. Patent No. 5,401,913) in view of either Bohn (U.S. Patent No. 6,537,412) or Johnston (U.S. Patent No. 5,153,050). Claims 8 and 10-13 were rejected under 35 U.S.C. 103(a) as obvious of Gerber et al. in view of either Bohn or Johnston and further in view of Daigle et al. (U.S. Patent No. 5,046,238). Claims 6, 7, and 14 were rejected under 35 U.S.C. 103(a) as obvious of Gerber et al. in view of either Bohn or Johnston or Gerber et al., Dangle et al. and either Bohn or Johnston, and further in view of Ikeda et al. (U.S. Patent No. 4,312,692). For the reasons discussed below, the Applicant requests the withdrawal of the obviousness rejections.

The basic requirements for establishing a *prima facie* case of obviousness as set forth in MPEP 2143 include (1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings, (2) there must be a reasonable expectation of success, and (3) the reference (or references when combined) must teach or

suggest all of the claim limitations. The Applicant submits that a *prima facie* case of obviousness cannot be established in the present case because the references, either taken singularly or in combination, do not teach or suggest all of the claim limitations.

Claim 1 of the present application recites a method of manufacturing a multilayer circuit board. The method comprises preparing a plurality of printed boards with respective copper foils, each printed board being made through the step of forming a via hole in an insulating substrate by laser processing from an insulating layer side so that the via hole extends in a direction of thickness of the insulating substrate so as to reach the conductive layer. The insulating substrate comprises a one-side copper-clad laminate wherein a plated conductor is formed in the via hole by electroplating using a copper foil as one electrode in a state in which the copper foil is covered by a protective film, a conductive bump is formed on the plated conductor, a bonding layer is formed at the insulating layer side, and the protective layer is stripped from the copper foil. The method further comprises etching the copper foil of at least one printed board, stacking the etched printed board and a second printed board, stacking an outermost conductor layer on the etched printed board with a bonding layer being interposed therebetween, and integrating the outermost conductor layer, the printed board with the conductor circuit, and the second printed board by one time of pressing and thereafter, etching the copper foils on opposite surfaces.

Claim 10 of the present application recites a method of manufacturing a multilayer circuit board comprising stacking printed boards with a bonding layer being interposed between the printed boards. Each printed board has a via hole extending through the

insulating substrate to the conductor layer, and the via hole is filled with a plated conductor by electroplating using a copper foil as one electrode in a state in which the copper foil is covered by a protective film. The plated conductor filling the via hole has an amount determined so that the plated conductor does not extend above the surface of the insulating substrate. The plated conductor is formed with a conductive bump extending through the bonding layer so that the conductive bump is connected to the conductor layer of another stacked printed board, and the protective layer is stripped from the copper foil. The method further comprises stacking an outermost conductor layer on an insulating layer side of a first outermost printed board with a bonding layer being interposed therebetween, and pressing the stack so that the printed boards and the outermost conductor layer are bonded together.

In the above methods recited in Claims 1 and 10, a plated conductor is formed in a via hole by electroplating using a copper foil as one electrode in a state in which the copper foil is covered by a protective film. The plated conductor is formed with a conductive bump, and the protective layer is stripped from the copper foil. The methods also include stacking and pressing processes to manufacture the multilayer circuit board. As will be discussed below the cited references, either taken singularly or in combination, fail to disclose or suggest such methods.

Since the plated conductor of the present invention is formed in the via hole in a state in which the copper foil is covered by a protective film, it is possible to minimize misregistration and distortion of the printed boards. In addition, the present invention allows for the uniform application of pressure over the entire surface of the printed boards when

performing the pressing operation, which allows a tip of a conductor bump of each of the printed boards to be surely electrically connected to a predetermined position of the conductor circuit of an adjacent printed board. Such a uniform application of pressure is possible because, since the electroplating is performed in a state in which the copper foil is covered by the protective film, plating does not deposit on the copper foil. Therefore, it is possible to always maintain a constant thickness of a conductor present on one surface of an insulating board (i.e. the thickness of the copper foil that originally has a fixed thickness) over the entire surface of the board, and the board does not warp.

If the conductor thickness varies in the board due to deposits on the copper foil, then the board will have a larger rigidity in a portion where the conductor thickness is larger and a smaller rigidity in a portion where the conductor thickness is small, and then the board will warp. If such warped printed boards with different conductor thicknesses are stacked, then the positions of the conductor bumps between the adjacent boards and the conductor circuits deviate from each other. As a result, reliable electric connection cannot be obtained. Such a situation is avoided by the methods of the present invention.

In addition, since the present invention advantageously provides a method that allows the conductor thickness of the printed boards to be fixed in each of the printed boards, then the thickness of the printed board including the insulating base material and the conductor can be fixed. Therefore, even if plural printed boards are stacked, a total board thickness of the plural printed boards in a sectional direction is uniform over the entire surface thereof. Consequently, it is possible to uniformly apply a pressure over the entire surface of the

printed boards when the press operation is performed. Thus, the tip of the conductor bump of each of the printed boards is electrically connected to a predetermined position of the conductor circuit of the adjacent printed board in a sure and reliable manner.

The Gerber et al. reference describes a method of manufacturing a multilayer circuit board as described below. An insulating layer is formed (e.g., see 10 of Fig. 1) and a conductor layer is formed on one side of the insulating layer (e.g., 12 of Fig. 2). Subsequently, plated resist is formed on the conductor layer (e.g., 14 of Fig. 3) and a plated conductor is formed in a portion where the plated resist is not formed (e.g., 16 of Fig. 4). Thereafter, a via hole reaching the conductor layer is formed (e.g., 18 of Fig. 5) (e.g., opening by laser) and a crown (a first conductive material) projecting from the surface of an insulating base material is provided in the via hole (20 of Fig. 6). Then, the plated resist (14) is removed, and the conductor layer (12) is etched to form a conductor circuit (e.g., 12 and 16 in Figs. 6 and 7). Moreover, a second conductive material is formed on the first conductive material (e.g., 22 in Fig. 8). Here, the second conductive material is a material having a low melting point.

Then, a bonding layer is placed on a conductive bump of each of one-side circuit boards (e.g., 24 of Fig. 9) and the one-side circuit boards are heated and pressed to obtain a multilayer circuit board.

The conductive layer on one side of the insulating board in the Gerber et al. reference is formed by evaporation and plating, while in the invention the protective film is bonded to the copper foil (which provides the benefits discussed above). The Gerber et al. reference

fails to disclose the use of a protective film covering the copper foil, in the manner expressly recited in Claims 1 and 10 of the present application. As discussed in detail above, the present invention advantageously provides a method that allows the conductor thickness to be fixed in the board, which is not possible with the Gerber et al. method. Consequently, distortion of each of the printed boards of the present invention can be minimized. Therefore, even if plural printed boards are laid one on top of another, the conductive bump and the conductor circuit are stacked between the adjacent printed boards without misregistration. Moreover, since fluctuation in a total board thickness of the plural printed boards can be minimized, it is possible to apply a pressure uniformly over the entire surface of the printed boards when the press operation is performed. Thus, the tip of the conductor bump of each of the printed boards is electrically connected to a predetermined position of the conductor circuit of the adjacent printed board in a sure and reliable manner.

Additionally, the Applicant submits that the Bohn and Johnston references fail to supplement the deficiency in the teachings of the Gerber et al. reference discussed above.

In the Bohn and Johnston references, plural double-sided circuit boards are stacked via an adhesive and heated and pressed to form a multilayer circuit board. In the Johnston reference, a copper foil is used as an outermost layer.

Here, the invention as claimed in the application concerned and Bohn and Johnston are compared. In the present invention, a via hole is formed and a plated conductor is formed in the via hole by electroplating a copper foil as one electrode in a state in which the copper foil is covered by a protective film. On the other hand, in the Bohn and Johnston references,

since a via hole is not formed, there is no plating step in which a copper foil is used as one electrode. Therefore, both the inventions of the Bohn and Johnston reference clearly do not teach or suggest a method where a plated conductor is formed in a via hole by electroplating using a copper foil as one electrode in a state in which the copper foil is covered by a protective film, the plated conductor is formed with a conductive bump, and the protective layer is stripped from the copper foil, as recited in Claims 1 and 10 of the present application.

Accordingly, the Applicant respectfully submits that a *prima facie* case of obviousness cannot be established with respect to Claim 1 of the present application. Thus, the Applicant respectfully requests the withdrawal of the obviousness rejection of Claim 1.

Claims 2-9 and 15 are considered allowable for the reasons advanced for Claim 1 from which they depend. These claims are further considered allowable as they recite other features of the invention that are neither disclosed nor suggested by the applied references when those features are considered within the context of Claim 1.

Regarding Claim 10, the Applicant submits that the Daigle et al. reference fails to supplement the deficiency in the teachings of the Gerber et al., Bohn, and Johnston references discussed above.

The Daigle et al. reference describes a method of manufacturing a multilayer circuit board as described below (see Figs. 1 to 7 and column 2, lines 29 to 46):

(1) forming circuits and pads on a removable mandrel;

(2) laminating layer of dielectric to the circuits and mandrel;

(3) forming an access opening at selected locations through the dielectric layer (using

laser, plasma, ion etch or mechanical drilling techniques) to expose selected circuit locations;

(4) forming conductive posts in the access openings to a level below the top of the access openings;

(5) providing fusible conductive material in the access opening; and

(6) removing the mandrel to obtain a one-side circuit board.

(7) Thereafter, a stack-up is made of a plurality of these discrete circuit layers. This stack-up is then subjected to heat and pressure to obtain a multilayer circuit board. Here, in the step (1), the circuits and the pads are formed by plating or evaporation as described in column 3, lines 58 to 62.

In the Daigle et al. reference a conductor layer on one side of an insulating board is formed by evaporation or plating, while in the present invention a protective film is provided on the copper foil, which provides the benefits discussed above (e.g., maintains the thickness of the copper foil, etc.). The Daigle et al. reference does not disclose such a protective film, and therefore conductor thickness is not maintained in the board. In fact, in Daigle et al. reference the mandrel is removed by etching or the like in order to obtain an independent conductor circuit. Since it is difficult to selectively remove only the mandrel with etching, fluctuation in the conductor thickness in the Daigle et al. reference tends to be large.

In addition, there is no indication in Daigle et al. that the rear side of the mandrel is covered by a protective film and a conductor circuit and a pad are formed on the mandrel.

Accordingly, the Applicant respectfully submits that a *prima facie* case of obviousness cannot be established with respect to Claim 10 of the present application. Thus,

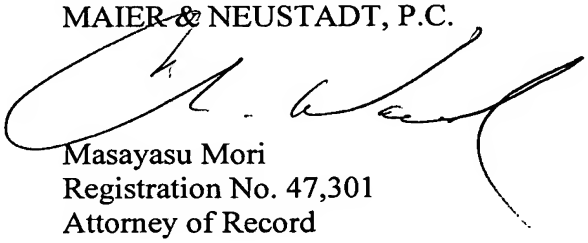
the Applicant respectfully requests the withdrawal of the obviousness rejection of Claim 10.

Claims 11-14 are considered allowable for the reasons advanced for Claim 10 from which they depend. These claims are further considered allowable as they recite other features of the invention that are neither disclosed nor suggested by the applied references when those features are considered within the context of Claim 10.

Consequently, in view of the above discussion, it is respectfully submitted that the present application is in condition for formal allowance and an early and favorable reconsideration of this application is therefore requested.

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



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